12/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02736783 SUPPLIER NUMBER: 107475148 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Hack-proofing options -- Best route to embedded CPU encryption depends on the app.
Arnaldo, Anthony
Electronic Engineering Times, 19
Sept 8, 2003
ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 496 LINE COUNT: 00045

... said Richard Chesson, ST's director of marketing for multimedia platforms. Similarly, ARM has new operating modes for its forthcoming ARM11 processor that act as **parallel** domains, but with a **different** privilege **level** .

To discourage **snooping** , MIPS has added the ability to "swizzle" information traveling between the **cache** and the core, making it impossible to decipher data by probing the **cache** line. There's also a way to randomly inject stalls into the core, scrambling the power signatures, said MIPS CTO Mike Uhler. This requires the...

12/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02713163 SUPPLIER NUMBER: 102205781 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Patent watch.
Microprocessor Report, 17, 4, 31(2)
April, 2003
ISSN: 0899-9341 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 1195 LINE COUNT: 00117

... architecture for providing explicit multithreading.

6,463,529: Compaq-Processor based system with system wide reset and partial system reset capabilities.

6,463,580: Intel- **Parallel** processing utilizing highly correlated data values.

Issued: October 1, 2002

6,460,115: IBM-System and method for **prefetching** data to **multiple levels** of **cache** including selectively using a software hint to override a hardware prefetch mechanism.

6,460,116: AMD-Using separate **caches** for variable and generated fixed-length instructions.

6,460,129: Fujitsu-Pipeline operation method and pipeline operation device to interlock the translation of instructions based...

12/3,K/3 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02277032 SUPPLIER NUMBER: 54068071 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Intel Turns Up The Heat : Pentium III shifts focus from price to performance.(Intel's Pentium III microprocessor)(Product Information)
Ristelhueber, Robert
Electronic News (1991), 45, 2258, 1(1)
Feb 22, 1999
ISSN: 1061-9577 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 831 LINE COUNT: 00064

... improve functions such as 3D graphics, where it has lagged AMD's 3Dnow technology. It also improved both the floating point and the way the **cache** works internally.

For its part, AMD has come up with TriLevel **Cache** to boost the performance of its new family. It consists of a 256KB **L2** write-back **cache** operating at the full speed of the processor, complementing the standard 64KB **L1** **cache** . It added a multiport internal **cache** design, enabling **simultaneous** 64-bit **reads** and writes to both the **L1** and **L2** **caches** . Finally, AMD added a 100MHz frontside bus to the external **cache** , which can serve as a scalable Level 3 **cache** on the motherboard.

The K6-III is positioned against the Pentium III, not the Pentium II, said Michael Steele, division marketing manager for the Computation...

12/3,K/4 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02273412 SUPPLIER NUMBER: 53969922 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Chips: AMD Introduces Industry-leading AMD-K6-III Processor With 3DNow! Technology. (Product Announcement)
EDGE: Work-Group Computing Report, NA
March 1, 1999
DOCUMENT TYPE: Product Announcement LANGUAGE: English
RECORD TYPE: Fulltext
WORD COUNT: 1280 LINE COUNT: 00106

TEXT:
...it is exceptionally fast. The backside 256KB L2 cache of the AMD-K6-III processor operates at full processor speed. For example, the internal L2 **cache** of an AMD-K6-III/450 processor operates at a full 450 MHz. The TriLevel **Cache** design also offers an internal multiport **cache** design. This flexible design feature delivers higher system performance by enabling **simultaneous** 64-bit **reads** and writes of both the **L1** **cache** and the **L2** **cache** . In addition, each **cache** can be accessed **simultaneously** by the processor core. The AMD-K6-III processor with 3DNow! technology incorporates AMD's TriLevel **Cache** design to enable leading-edge performance for today's consumer PC enthusiasts and business power users. The 21.3-million transistor AMD-K6-III processor...

12/3,K/5 (Item 5 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02271380 SUPPLIER NUMBER: 53939875 (USE FORMAT 7 OR 9 FOR FULL TEXT)
AMD ANTICIPATES PENTIUM III LAUNCH WITH THE K6-III.
Computergram International, NA
Feb 23, 1999
ISSN: 0268-716X LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 388 LINE COUNT: 00031

TEXT:
...cache, more than any other x86 CPU, and up to 1,344Kb in total. No other x86-compatibles have the option of an external L3 **cache** on the motherboard. In comparison, the Pentium III has 32Kb of internal **cache** and up to 512Kb of half-speed external L2 **cache** , a total of 512Kb. AMD says its **Level 2 cache** also runs at full processor clock speeds, and that the design incorporates internal multiport **caching** , so that **simultaneous** 64-bit **reads** and writes of both the **L1** and **L2** **caches** are enabled. Compaq said it planned to use the new chips in a faster version of its Presario internet PCs. The 0.25 micron, 21...

12/3,K/6 (Item 6 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02251605 SUPPLIER NUMBER: 53380936 (USE FORMAT 7 OR 9 FOR FULL TEXT)
K7 Challenges Intel. (AMD K7 processor) (Product Development)
Microprocessor Report, 12, 14, NA

Oct 26, 1998
ISSN: 0899-9341 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 5460 LINE COUNT: 00410

... the queue, the store's data is forwarded to the load as soon as it becomes available, thus allowing the load to complete without a **cache** access.

The cache is nonblocking, so when an L1 miss goes to the **L2** or the bus for resolution, other loads behind it in the queue can access the cache. The data cache has three complete sets of tags, allowing **simultaneous** tag **lookup** by two requests from the queue and a **snoop** from the bus.

The data cache is physically tagged. Effective addresses are translated to physical addresses in **parallel** with D-cache tag **lookup** by a **two - level** translation lookaside buffer (TLB). The **first level** has 32 fully associative entries and is backed by a 256-entry, four-way set-associative **second level** . The memory mapper supports both the 4K and 4M page sizes of Intel's 36-bit physical-address-space extension and the newer extended server...

12/3,K/7 (Item 7 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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02036309 SUPPLIER NUMBER: 19054544 (USE FORMAT 7 OR 9 FOR FULL TEXT)
High-performance PC servers. (storage and memory terms) (Lan Glossary) (Technology Information)(Column)
Zeichick, Alan
LAN Magazine, v12, n2, p138(1)
Feb, 1997
DOCUMENT TYPE: Column ISSN: 1069-5621 LANGUAGE: English
RECORD TYPE: Fulltext
WORD COUNT: 889 LINE COUNT: 00070

... as the primary working memory for most PCs.

FPM RAM Fast Page Mode RAM is an older standard for primary working memory. FPM RAM cannot **simultaneously** seek and **retrieve** memory locations, and it has been largely replaced by extended data output RAM.

L1 Cache A very small, very fast static RAM **cache** , **Level - 1 Cache** is located within the processor chip itself. For example, the Intel Pentium CPU has 16Kbytes of **L1 Cache** .

L2 Cache An external static RAM-based **cache** , **Level - 2 Cache** helps feed memory contents to the main processor, which it does faster than DRAM, by preloading expected addresses. Typical **L2 Cache** sizes are between 256KB and IMB. L2 **Caches** typically have either a pipeline-burst design or a faster, flow-through design.

Cache RAM **Cache** is a small pool of high-speed memory that stores data likely to be requested next by the processor. See **L1 Cache** , **L2 Cache** .

SRAM Unlike DRAM, Static RAM "remembers" bits without having to be constantly refreshed. It is faster than DRAM, but more expensive. It is typically used for **L2 caches** .

SDRAM **Synchronized** Dynamic RAM is an emerging replacement for DRAM. SDRAM's memory access cycles are **synchronized** with the main processor's clock to eliminate the processor's wait time between memory **fetches** .

12/3,K/8 (Item 8 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01982298 SUPPLIER NUMBER: 18627015 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Pentium desktops just got faster. (evaluation of four Pentium-based PCs) (includes related article on Universal Serial Bus design, and benchmarks used in testing) (Hardware Review) (Evaluation)
Lamm, Roger
PC User, n286, p28(4)

June 26, 1996
DOCUMENT TYPE: Evaluation ISSN: 0263-5720 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 4039 LINE COUNT: 00302

... 430HX (formerly the Triton II). The 430VX supports synchronous dynamic RAM (SDRAM) and Concurrent PCI technology, which enables PCI and ISA buses to execute transactions **simultaneously** with no lag time.

The 430HX supports **Concurrent** PCI, error **checking** and correcting (ECC) memory, **dual** processing and a shared second **level cache** that maximises EDO RAM. It also supports Unified Memory Architecture, which eliminates the need for dedicated display memory (PC User, 17 April 1996).

The 430VX...

12/3,K/9 (Item 9 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01932208 SUPPLIER NUMBER: 18241364 (USE FORMAT 7 OR 9 FOR FULL TEXT)
200MHz Pentium PCs on the horizon. (Gateway 2000's P5-200 PC, IBM's PC 300, Dell Computer's Dimension, HP's Vectra VL and NEC's PowerMate) (Product Announcement)
Dicarlo, Lisa
PC Week, v13, n17, p1(2)
April 29, 1996
DOCUMENT TYPE: Product Announcement ISSN: 0740-1604 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 504 LINE COUNT: 00046

... Unlike the others, NEC will incorporate Intel's 430HX chip set and [illegible] Intel motherboard, code-named Cumberland, according to sources.

The 430HX supports **Concurrent** PCI, error- **checking** and-correcting memory, **dual** processing and a shared **Level** 2 **cache** that maximizes extended Data Out RAM. Advanced PCs will be equipped with pipeline burst **cache** .

Officials from Gateway 2000, Dell, IBM, HP, NEC and Intel declined to comment on unannounced products.

Speed Thrills: 200MHz desktop PCs due in June

Vendor...

12/3,K/10 (Item 10 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01776608 SUPPLIER NUMBER: 16890160 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Hal reveals multichip SPARC processor. (Hal Computer Systems' Sparc64) (includes related article on price and availability)
Gwennap, Linley
Microprocessor Report, v9, n3, p1(7)
March 6, 1995
ISSN: 0899-9341 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 4518 LINE COUNT: 00350

... speeds branch handling.

The fetch unit takes up to four instructions per cycle from the [illegible] buffer. If the needed data is not in the **prefetch** buffer (due to a misprediction), the **fetch** unit can instead **read** the data from the L1 **cache** with no delay. The L1 **cache** is nonblocking and capable of providing data at the **same time** that it is accepting data from the **prefetch** buffer. If an access misses the **L1 cache** as well, the needed instructions must be **fetched** from the **L2 cache** , requiring a delay of three cycles. The deep queues in the execution engine typically mask this delay.

As long as instructions are available, the fetch unit will read four arbitrarily aligned instructions and pass them to the issue unit. The only exception occurs if the end of a **cache** line is reached; because the fetch

unit cannot access two cache lines at once, it will finish one line, then begin the next line on...

12/3,K/11 (Item 11 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01494864 SUPPLIER NUMBER: 11772876 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Storage Technology announcements: Storage Technology makes its case for Iceberg being the disk technology for the 1990s. (Product Announcement)
Computergram International, n1848, pCGI01310007
Jan 31, 1992
DOCUMENT TYPE: Product Announcement ISSN: 0268-716X LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 1059 LINE COUNT: 00090

... be data transfers. The controller has eight Am29000 control processors which simultaneously process channel programs on eight separate channels. On the back end of the **cache** , XSA supports 16 unidirectional data paths to the disk arrays, eight in each direction. Two are dynamically assigned for status and control, and the other 14 are used for transferring compressed data. This parallel design enables XSA to stage and de-stage data between the **cache** and any 14 devices **simultaneously** and independently of channel activity. **Each** device has an actuator **level** buffer used for **reading** and writing.

Extended Performance Capabilities

XSA uses **caching** techniques, non-volatile storage and actuator-level buffers to eliminate synchronous data transfers to and from physical devices. It is optimised for writing to disk...

12/3,K/12 (Item 12 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01450210 SUPPLIER NUMBER: 11226249 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Bits & PCs: your guide to all the latest and best PC products.
PC User, n165, p28(3)
August 14, 1991
ISSN: 0263-5720 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 1011 LINE COUNT: 00081

... DAS 2 is a new anti-hacking device from Kerridge Network Systems. It sits between the host computer and the modem and provides up to **two** secure ports.

Features include four- **level** password security and **call** monitoring for both **synchronous** and asynchronous services.

Units can be added in a cascading system to provide up to 64 ports. BT charge rates can be set to monitor calls. 1,395 pounds Fast facts: 297

Compatibles

* PC340 * Ti'Ko * (0506) 857666

Ti'Ko's latest 40MHz 386-based computer has a 128Kb **cache** and offers users a 43Mb hard disk, 3 1/2-inch and 5 1/4-inch floppy disk drives and a SuperVGA monitor. Other hard...

12/3,K/13 (Item 13 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
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01204305 SUPPLIER NUMBER: 04635102 (USE FORMAT 7 OR 9 FOR FULL TEXT)
32-bit microprocessors. (1987 technology forecast)
Bursky, Dave
Electronic Design, v35, p128(8)
Jan 8, 1987
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 4367 LINE COUNT: 00333

... giving way to Harvard-type structures, which do more things in parallel, thus improving system efficiency. Multiple 32-bit address and data buses, on-chip **caches** for instructions and data, embedded memory-management units, and translation **look** -aside buffers operate in **parallel** with the CPU, thanks to large instruction queues and **multiple** [illegible] **levels** . The higher degree of parallelism cuts the execution time per instruction, raising throughout.

Large on-chip register files -- from hundreds to thousands of bytes ...

12/3,K/14 **(Item 1 from file: 621)**
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)
(c) 2004 The Gale Group. All rts. reserv.

01813283 Supplier Number: 53925031 (USE FORMAT 7 FOR FULLTEXT)
AMD Introduces Industry-leading AMD-K6-III Processor With 3DNow! Technology.
Business Wire, p1254
Feb 22, 1999
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 1415

... it is exceptionally fast. The backside 256KB L2 cache of the AMD-K6-III processor operates at full processor speed. For example, the internal L2 **cache** of an AMD-K6-III/450 processor operates at a full 450 MHz.

The TriLevel **Cache** design also offers an internal multiport **cache** design. This flexible design feature delivers higher system performance by enabling **simultaneous** 64-bit **reads** and writes of both the **L1 cache** and the **L2 cache** . In addition, each **cache** can be accessed **simultaneously** by the processor core.

About the AMD-K6(R)-III Processor

The AMD-K6-III processor with 3DNow! technology incorporates AMD's TriLevel **Cache** design to enable leading-edge performance for today's consumer PC enthusiasts and business power users. The 21.3-million transistor AMD-K6-III processor...

12/3,K/15 **(Item 1 from file: 636)**
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

04178834 Supplier Number: 54690614 (USE FORMAT 7 FOR FULLTEXT)
Better and Faster: Technology Pushes Storage.
Ochiva, Dan
Millimeter, pNA
April, 1999
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Newsletter; Trade
Word Count: 3437

... offers SCSI Fast-Wide/Ultra-Wide and/or Fibre Channel connections. Other features include pro-OS (process-optimized Operating System), fifth-generation storage management software, **read** -ahead/write-behind data **caching** (speeds I/O), partitionable data storage space, and **multiple / concurrent** RAID **levels** 0, 1, and 5.

Alpharetta, Georgia-based Raidtec offers RAIDserver, another NAS-type [illegible] rack line. The company claims that the server offers improved [illegible]...

12/3,K/16 **(Item 2 from file: 636)**
DIALOG(R)File 636:Gale Group Newsletter DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

04119943 Supplier Number: 53956779 (USE FORMAT 7 FOR FULLTEXT)
AMD: AMD introduces industry-leading AMD-K6-III processor with 3DNow! technology.
M2 Presswire, pNA
Feb 23, 1999
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 1309

... it is exceptionally fast. The backside 256KB L2 cache of the AMD-K6-III processor operates at full processor speed. For example, the internal L2 **cache** of an AMD-K6-III/450 processor operates at a full 450 MHz. The TriLevel **Cache** design also offers an internal multiport **cache** design. This flexible design feature delivers higher system performance by enabling **simultaneous** 64-bit **reads** and writes of both the **L1 cache** and the **L2 cache** . In addition, each **cache** can be accessed **simultaneously** by the processor core. About the AMD-K6-III Processor
The AMD-K6-III processor with 3DNow! technology incorporates AMD's TriLevel **Cache** design to enable leading-edge performance for today's consumer PC enthusiasts and business power users. The 21.3-million transistor AMD-K6-III processor...

12/3,K/17 **(Item 1 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2004 The Gale Group. All rts. reserv.

06906882 Supplier Number: 57929482 (USE FORMAT 7 FOR FULLTEXT)
CompactPCI CT Resources.
Grigonis, Richard
Computer Telephony, v7, n11, p97
Nov, 1999
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 5833

... Unlike some other systems on the market, Lucent's CPCI Speech Processing Board comes with the right to use its speech software without having to **obtain** individual licenses for each set of channels.
The 6U high cPCI board is hot-swappable. The 32-bit bus handles a 133 MBPS data bandwidth. Three RISC processors with **1** MB **Level 2 caches** are used (instead of DSPS) that sit on 64-bit memory buses. The board holds 192 MB of SDRAM and supports 128 **simultaneous** channels. You'll **find** available onboard: 64 **simultaneous** channels of echo cancellation, 64 simultaneous channels of text-to-speech, 64 simultaneous channels compressed speech (16 bit linear LCCELP, ADPCM, mu-law or a...

12/3,K/18 **(Item 2 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)
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04609046 Supplier Number: 46779729 (USE FORMAT 7 FOR FULLTEXT)
Fujitsu lights fire under Sparc CPU
Electronic Engineering Times, p146
[illegible], 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 564

... to its tag bits, process identifier bits, allowing lines to be invalidated by process to avoid a complete flush on a context switch. The data **cache** operates in copy-back mode with a write buffer, keeping the level of bus activity down. Both caches use streaming loads, so that a request that triggers a **cache** miss is met directly from the **L2 cache** , without waiting for the **L1** line to fill.
The **L2 cache** also shows some interesting design ideas. It is direct-mapped, but write-through, rather than write-back. The on-chip **L2**

controller manages the **cache** as a **look** -aside unit, sharing a common data bus with main memory. Thus, on an **L1** miss, the chip automatically starts both a DRAM access and an **L2** access, and aborts the DRAM cycle if the **L2** **cache** has the data. Using Fujitsu 32k-by-36 **synchronous** SRAMs, the **cache** line is four 64-bit words, contained in four 72-bit **cache** entries. The additional bits include two parity bits and the tag information. The L2 controller thus picks up the data and tag information in the...

12/3,K/19 **(Item 3 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2004 The Gale Group. All rts. reserv.

04324468 Supplier Number: 46339075 (USE FORMAT 7 FOR FULLTEXT)
200MHz Pentium PCs on the horizon
PC Week, p001
April 29, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Tabloid; General Trade
Word Count: 509

... Unlike the others, NEC will incorporate Intel's 430HX chip set and a second Intel motherboard, code-named Cumberland, according to sources.

The 430HX supports **Concurrent** PCI, error- **checking** and-correcting memory, **dual** processing and a shared **Level** 2 **cache** that maximizes Extended Data Out RAM. Advanced PCs will be equipped with pipeline burst **cache** .

Officials from Gateway 2000, Dell, IBM, HP, NEC and Intel declined to comment on unannounced products.

Speed Thrills: 200MHz desktop PCs due in June

Vendor...

12/3,K/20 **(Item 4 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)
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01169340 Supplier Number: 41925164 (USE FORMAT 7 FOR FULLTEXT)
Secondary cache aids R4000 hit rate
Electronic Engineering Times, p102
March 11, 1991
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 581

... The access time of the R4000 secondary cache is programmable as an integral number of processor clock cycles to support SRAMs of varying speeds. Larger **caches** can be built with slower and less expensive SRAMs, and the processor clock speed can be increased without affecting the secondary-cache design. The designer can therefore target various price/performance levels.

O/S considerations

While virtually indexed, physically tagged caches allow **parallel** **cache** **interrogation** and translation **look** -aside buffer (TLB) **lookup** , physical **caches** simplify sharing of data with different virtual addresses. The R4000 incorporates virtually indexed **first - level** **cache** and physically tagged and indexed **second - level** **cache** to eliminate "aliasing problems," which add complexity to the operating-system software.

For maintaining coherency among private **caches** in a bus-based multiprocessing system, snooping must be carried out in the secondary **cache** . The proper subset property must be maintained between the first and second **cache** levels. The R4000 maintains that subset property and cache coherency by keeping the cache state information (dirty, shared, etc.) in both the first- and second...

12/3,K/21 (Item 5 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)
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01134507 Supplier Number: 41872721 (USE FORMAT 7 FOR FULLTEXT)
Emulator enhanced: SUPPORTS MOTO'S 32-BIT COPROCESSOR
Electronic Engineering Times, p60
Feb 18, 1991
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 196

... a highly graphical user interface. The interface is flexible; designers can move windows or resize them at will. With the floating-point capability, designers can **look** at register or memory contents in floating-point formats.

Other standard features include support for **cache** bursts and **synchronous** cycles, **both** source-and symbolic- **level** debugging, and zero-wait-state high-speed RAM overlay.

Pricing for the development system starts at $30,000.

Jay Maggard, (206) 882-2000

Reader Service...

12/3,K/22 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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[illegible] SUPPLIER NUMBER: 60598141 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Novel Architectures, Parallelism Rule The Roost In Digital Circuits.
[illegible]PY, DAVE
Electronic Design, 48, 5, 142
March 6, 2000
ISSN: 0013-4872 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 2445 LINE COUNT: 00196

... and double-extended data types. The main datapath consists of a 10-stage core pipeline that can execute up to six IA-64 instructions in **parallel** during each clock cycle. A large on-chip register file provides programmers with 128 integer, 128 floating-point, 64 one-bit predicate, and eight branch registers (Fig. **1**). **Level - 1** and **level - 2** caches are integrated on the chip. A level-3 cache interface can address up to 4 Mbytes over a dedicated back-side bus that employs a source- **synchronous** interface. **Both level - 2** and -3 caches include error **checking** and correction to ensure data integrity.

The processor was designed to handle multiple operations in parallel, so it includes these 11 execution units: four integer...

12/3,K/23 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2004 The Gale Group. All rts. reserv.

[illegible]0244901 SUPPLIER NUMBER: 20768235 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Optimized for digital video and audio, CPU uses new 3DNow instruction set -- AMD hopes K6-2 chip puts it back in games. (Product Information)
[illegible]ammers, David
Electronic Engineering Times, n1011, p34(1)
June 8, 1998
ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 949 LINE COUNT: 00073

... second half.

By the end of 1998, AMD will offer the K6-3 product line with a superscalar instruction set and nearly double the K6- **2** 's **Level 1 cache** . It will be positioned against Intel's Katmai processor. AMD officials added that the K-7 would be **ready** at about the **same time** Intel's Merced hits the market, but that was before Intel's May 29

announcement of delays in the Merced schedule.
Herb lectured about 100...

12/3,K/24 (Item 3 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2004 The Gale Group. All rts. reserv.

08273850 SUPPLIER NUMBER: 17618004 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Do 'asynchronous cache' and 'pipeline burst cache' sound like Greek? Read on.(question-and-answer) (Help Desk)(Column)
Glass, Brett
InfoWorld, v17, n46, p58(1)
Nov 13, 1995
DOCUMENT TYPE: Column ISSN: 0199-6649 LANGUAGE: English
RECORD TYPE: Fulltext
WORD COUNT: 703 LINE COUNT: 00055

... information from the Level 2 cache.
If the external cache doesn't contain the required data, it makes little difference what kind the Level 2 **cache** is; the motherboard chip set must do a slow and arduous fetch from main memory. But if the external **cache** does contain the needed data, it must send it to the CPU in a rapid burst of four or more chunks. (This operation is often **called** a burst fill because it fills the **Level 1 cache** from the **Level 2 cache** .) This is when external **cache** architecture makes a difference.
A **synchronous** external **cache** can always furnish data as fast as the CPU asks for it. This is the fastest kind, but it requires superfast RAM and is therefore very expensive. Second best is a pipelined burst **cache** . This type of **cache** takes a bit longer than a synchronous **cache** to retrieve the first chunk of data but prepares the next while the previous one is being sent so that no time is lost after...

12/3,K/25 (Item 4 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
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07621804 SUPPLIER NUMBER: 16735645 (USE FORMAT 7 OR 9 FOR FULL TEXT)
PowerPC flagship sets sail.
Wilson, Richard
Electronics Weekly, n1698, p14(1)
Oct 19, 1994
ISSN: 0013-5224 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 662 LINE COUNT: 00051

... 16-word data block can be copied to the write-back buffer.
The architecture defines the unit of coherency as a 64byte (16-word) line **cache** block. To ensure **cache** coherency the data **cache** supports the four-state MESI (modified/exclusive/shared/invalid) protocol.
Another feature which separates the 620 from its predecessors is the use of an on-chip **L2 cache** controller which supports configurations from 1Mbyte to 128Mbyte using the same 64byte block size as the internal **L1 caches** . The **L2 cache** is a direct-mapped error correction code protected unified instruction and secondary data **cache** . It supports the use of single and double register **synchronous** SRAMs and the **L2** interface supports a number of external SRAM access speeds as well as an external coprocessor, and the direct-mapped error correction code.
It is a superscalar microprocessor which **fetches** , dispatches and completes up to four instructions per cycle. In order to keep its multiple pipelines flowing the 620 uses the prediction of branch instructions...

12/3,K/26 (Item 5 from file: 148)
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0[illegible]419 SUPPLIER NUMBER: 16507314 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Traditional CISC CPUs and MPUs move toward RISC to boost performance. (complex instruction set computer; central processing unit; microprocessing unit; reduced instruction set computer)
[illegible], Dave
[illegible] Design, v42, n25, p39(4)
[illegible], 1994
[illegible]-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 3128 LINE COUNT: 00244

... Nx586 processor delivers higher throughputs than the Intel Pentium when running at the same clock speeds. The secret is a RISC core combined with a **second - level cache** controller, 16-kbyte data and instruction **caches** (four-way set associative), and a proprietary coprocessor interface to an off-chip floating-point unit. Its **fetch** stack allows four **simultaneous level - 2** to **level - 1 cache** replacements. In addition, a write-reservation queue supports out-of-order instruction execution and in-order retirement, which helps maximize software throughput.
By using a...

12/3,K/27 **(Item 6 from file: 148)**
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04601829 SUPPLIER NUMBER: 08581886 (USE FORMAT 7 OR 9 FOR FULL TEXT)
ACI bus supports 486 multiprocessing; S3's cache controllers use MESI protocol. (Advanced Chip Interconnect) (Modified, Exclusive, Shared, Invalid) (technical)
Thorson, Mark
Microprocessor Report, v4, n11, p9(3)
[illegible] 10, 1990
[illegible]MENT TYPE: technical ISSN: 0899-9341 LANGUAGE: ENGLISH
[illegible] TYPE: FULLTEXT
[illegible] COUNT: 1976 LINE COUNT: 00157

... the processor only on a snoop hit. On a snoop miss, it is guaranteed that the cycle does not affect data in the first-level **cache** , so it is unnecessary to propagate the cycle. This shields the processor from the heavy bus traffic typical of multiprocessor systems.
Guaranteed inclusion is implemented...

...in the second-level cache, or when both the first- and second-level caches are being loaded simultaneously from system memory. This ensures that the **first - level** cache can only obtain data present in the **second - level** cache. Invalidation cycles are run on the **first - level** cache whenever data is invalidated or replaced in the **second - level** cache. This ensures that data will not persist in the **first - level** cache after it has ceased to exist in the **second - level** cache. It also couples the **first - level** cache to the MESI coherency protocol implemented among the **second** -level caches, which ensures system-wide **cache** coherency.
Conclusion
The S3 chip set is an elegant solution for Intel-based multiprocessor systems. The S3 design provides the necessary features in a form...

12/3,K/28 **(Item 1 from file: 15)**
[illegible]DIALOG(R)File 15:ABI/Inform(R)
[illegible]4 ProQuest Info&Learning. All rts. reserv.

[illegible]: 99-68411
Fujitsu lights fire under Sparc CPU
[illegible]son, Ron
Electronic Engineering Times n922 PP: 146 Oct 7, 1996
ISSN: 0192-1541 JRNL CODE: ELET
WORD COUNT: 561

...TEXT: to its tag bits, process identifier bits, allowing lines to be invalidated by process to avoid a complete flush on a context switch. The

data **cache** operates in copy-back mode with a write buffer, keeping the level of bus activity down. Both caches use streaming loads, so that a request that triggers a **cache** miss is met directly from the **L2** **cache** , without waiting for the **L1** line to fill.

The **L2** **cache** also shows some interesting design ideas. It is direct-mapped, but writethrough, rather than write-back. The on-chip **L2** controller manages the **cache** as a **look** -aside unit, sharing a common data bus with main memory. Thus, on an **L1** miss, the chip automatically starts both a DRAM access and an **L2** access, and aborts the DRAM cycle if the **L2** **cache** has the data. Using Fujitsu 32k-by36 **synchronous** SRAMs, the **cache** line is four 64-bit words, contained in four 72-bit **cache** entries. The additional bits include two parity bits and the tag information. The L2 controller thus picks up the data and tag information in the...

12/3,K/29 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
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01266668 CMP ACCESSION NUMBER: EET20030908S0019
Hack-proofing options - Best route to embedded CPU encryption depends on the app
Anthony Cataldo
ELECTRONIC ENGINEERING TIMES, 2003, n 1286, PG19
PUBLICATION DATE: 030908
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Feature
WORD COUNT: 461

... said Richard Chesson, ST's director of marketing for multimedia platforms. Similarly, ARM has new operating modes for its forthcoming ARM11 processor that act as **parallel** domains, but with a **different** privilege **level** .

To discourage **snooping** , MIPS has added the ability to "swizzle" information traveling between the **cache** and the core, making it impossible to decipher data by probing the **cache** line. There's also a way to randomly inject stalls into the core, scrambling the power signatures, said MIPS CTO Mike Uhler. This requires the...

12/3,K/30 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
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01163642 CMP ACCESSION NUMBER: EET19980608S0045
Optimized for digital video and audio, CPU uses new 3DNow instruction set - AMD hopes K6-2 chip puts it back in games
David Lammers
ELECTRONIC ENGINEERING TIMES, 1998, n 1011, PG34
PUBLICATION DATE: 980608
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Business
WORD COUNT: 870

... second half.

By the end of 1998, AMD will offer the K6-3 product line with a superscalar instruction set and nearly double the K6- **2** 's **Level** **1** **cache** . It will be positioned against Intel's Katmai processor. AMD officials added that the K-7 would be **ready** at about the **same** **time** Intel's Merced hits the market, but that was before Intel's May 29 announcement of delays in the Merced schedule.

Herb lectured about 100...

12/3,K/31 (Item 3 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
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01196083 CMP ACCESSION NUMBER: EET19961007S0183
Fujitsu lights fire under Sparc CPU
Ron Wilson
ELECTRONIC ENGINEERING TIMES, 1996, n 922, PG146
PUBLICATION DATE: 961007
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: News
WORD COUNT: 571

... flush on a context switch. The data cache operates in copy-back mode with a write buffer, keeping the level of bus activity down. Both **caches** use streaming loads, so that a request that triggers a **cache** miss is met directly from the L2 **cache** , without waiting for the L1 line to fill.

The L2 **cache** also shows some interesting design ideas. It is direct-mapped, but write-through, rather than write-back. The on-chip **L2** controller manages the **cache** as a **look** -aside unit, sharing a common data bus with main memory. Thus, on an **L1** miss, the chip automatically starts both a DRAM access and an **L2** access, and aborts the DRAM cycle if the **L2** **cache** has the data. Using Fujitsu 32k-by-36 **synchronous** SRAMs, the **cache** line is four 64-bit words, contained in four 72-bit **cache** entries. The additional bits include two parity bits and the tag information. The L2 controller thus picks up the data and tag information in the...

12/3,K/32 (Item 4 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
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00588718 CMP ACCESSION NUMBER: EET19910218S1605
SUPPORTS MOTO'S 32-BIT COPROCESSOR - Emulator enhanced
STAN RUNYON
ELECTRONIC ENGINEERING TIMES, 1991, n 629, 60
PUBLICATION DATE: 910218
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Design - Test & Measurment
WORD COUNT: 197

... a highly graphical user interface. The interface is flexible; designers can move windows or resize them at will. With the floating-point capability, designers can **look** at register or memory contents in floating-point formats.

Other standard features include support for **cache** bursts and **synchronous** cycles, **both** source- and symbolic- **level** debugging, and zero-wait-state high-speed RAM overlay.

Pricing for the development system starts at $30,000.

Jay Maggard, (206) 882-2000

12/3,K/33 (Item 5 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
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00588623 CMP ACCESSION NUMBER: EET19910311S1510
Secondary cache aids R4000 hit rate
ASHIS KHAN
ELECTRONIC ENGINEERING TIMES, 1991, n 632, 102
PUBLICATION DATE: 910311

JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Design
WORD COUNT: 595

... The access time of the R4000 secondary cache is programmable as an integral number of processor clock cycles to support SRAMs of varying speeds. Larger **caches** can be built with slower and less expensive SRAMs, and the processor clock speed can be increased without affecting the secondary-cache design. The designer can therefore target various price/performance levels.

O/S considerations

While virtually indexed, physically tagged caches allow **parallel cache interrogation** and translation **look** -aside buffer (TLB) **lookup** , physical **caches** simplify sharing of data with different virtual addresses. The R4000 incorporates virtually indexed **first - level cache** and physically tagged and indexed **second - level cache** to eliminate " aliasing problems," which add complexity to the operating-system software.

For maintaining coherency among private **caches** in a bus-based multiprocessing system, snooping must be carried out in the secondary **cache** . The proper subset property must be maintained between the first and second **cache** levels. The R4000 maintains that subset property and cache coherency by keeping the cache state information (dirty, shared , etc.) in both the first- and second...